In the Specification:

Please replace the last paragraph, which begins on page 20 and ends on page 22, beginning at line 12 of page 20, with the following rewritten paragraph.

The CAM memory array 70 also includes a key field row and column input port 76 that are coupled to a write address register 110. The write address register 110 receives inputs, namely the row and column (i.e. the CAM physical address), to write a K+N bit word during a CAM write cycle. As part of the write operation, the address generation logic 120 supplies the next CAM address in the memory array to be used. Further control of the address generation logic 120 is accomplished via a number of control lines which are necessary for the management of the addressing in the write modes and are under control of the Packet Buffer Access Controller 25. In the write mode, the 2:1 address mux 125 accepts the same row and column address driven into port 76 for accessing the key field for accessing the associated N-bit association field through port 77. When the write is commanded via ~~Read/write~~read/write strobe control 150, the contents of the K+N bit data write register are placed into the proper K and N bit fields through ports 72 and 73 CAM memory 70 to the location selected by the row and column addresses supplied on ports 76 and 77.To control the mux mode a R/W Mode (i.e. read/write mode) control line is used. This signal could be generated by the Packet Buffer Access Controller 25. When it is desired to read from the array, the 2:1 mux 125 selects the output of the Read Address Register 140 under control of the R/W Mode line. Register 140 accepts as input the row and column address of the key matching the key input previously stored in 80. The Read Address Register is "loaded" when the Key Match line 79 is asserted. This occurs when the key loaded into 80 identically matches a key field in the CAM memory array. Additionally this

information, the key row and column from port 78 and the key match condition indicated from port 79, are used by the Address Generation Logic 120 to track locations to be freed as they are individually accessed in the ~~in the~~ CAM array 70. Each time an N-bit key matches the [a] new key input on port 71 the CAM array location is to be freed for overwriting at some later time as deemed necessary under the rules designed into the address generation logic 120. Continuing in the read operation, the N bit data stored in the row and column address pointed to by the Read Address Register 140 is fed through the 2:1 mux 125 into the Association Row and Column port 77. The result is that the desired N-bit association data will be output on 75 of the memory array 78. The Association Readout port 75 is coupled to the Association Compare Register 100. The register holds the N-bit data (which is the address of the next packet to be read from the Output Packet Buffer 30) for a second search to determine if any other instances of the current N-bit association field exist in the memory array. If they do then the packet has not been served to all the ports and the multicast is not complete. In this case the Association Match port 88 of the Memory Array 70 is not asserted. The Association Match line 88 is used to control the FREE indicator 56. In other words, if no Association match occurs during a second read (i.e. Association Match is low), then the current address can now be marked as available, and placed into the FAT 60 by asserting the FREE line 56 from the Dual Key CAM 50. Returning to the compare mode, under control from the Packet Buffer Access Controller 25, the Association Compare Register is loaded with the current output of port 88 when the LOAD 1 line is asserted. The contents of 100 are then applied to the CAM memory array 70 through port 74 to search for exact N-bit matches in each N-bit association field. Thus the association field from the first search to look-up a new packet address, has become a key to search for other remain instances of the same address. This is the dual

key operation. In the search for "yet to be serviced" multicast outputs only an indication of the presence of instances of the address is required, hence the single line Association Match output port 88.

Please replace the paragraph bridging pages 26 and 27, beginning at line 24, with the following rewritten paragraph.

The X node 321 is coupled to the gates of row address transistors T5 and T6, which have their source-drain paths coupled between respective data nodes D and D BAR and complementary Data and Data BAR lines 331 and 332. The Data and Data BAR lines 331 and 332 are coupled to other memory cells of the same Y column of the memory array. The Y node 322 is coupled to the gates of column address transistors T7 and T8, which have their source-drain paths respectively coupled in circuit with the source-drain path of a data input (or write) transistor T9 and a data output (or read) transistor T10.